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PATENT APPLICATION

ATTORNEY DOCKET NO. 10001846-1

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Krech et al.

Serial No.: 09/659,256 **Examiner:** Shrader

Filing Date: Sept 11, 2000 **Group Art Unit:** 2124

Title: Method and Apparatus for No-Latency Conditional Branching

ASSISTANT COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in triplicate is the Appeal Brief in this application with respect to the Notice of Appeal filed on **Oct 30, 2003**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $330.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$420.00
( )	three months	$950.00
( )	four months	$1480.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 50-1078 the sum of **$330.00**. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 50-1078 pursuant to 37 CFR 1.25.

(X) A duplicate copy of this transmittal letter is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 222313-1450.
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I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.
( ) Date of Facsimile:

Typed Name: **June L. Bouscaren**
Signature: June L. Bouscaren

Respectfully submitted,

Krech et al.

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Docket No. 10001846-1
USPTO Ser. No. 09/659,256

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Matter of the Application of: Krech et al.
Serial No.: 09/659,256
Filed: September 11, 2000
For: Method and Apparatus for No-Latency Conditional Branching
Examiner: Shrader
Group Art Unit: 2124

Assistant Commissioner for Patents
Washington, DC 20231

Appeal Brief

Real party in Interest: Agilent Technologies, Inc.

Related Appeals and Interferences: There are no related appeals and interferences.

Status of Claims: Claims 1-11 and 15-18 are rejected. Claims 12-14 are allowed.

Status of Amendments: Amendments to the Abstract will be entered upon submission of this Appeal Brief. See Paper No. 7, page 2.

Summary of the Invention: An apparatus that performs conditional branching has a sequencer for executing program instructions including a conditional branch instruction specifying a branch condition address 300 and a conditional instruction. See Specification p. 17, line

30 through p.18, line 6. The apparatus also has a branch unit 302 including a programmable flag selection memory 502 and a plurality of first flag selectors 504. See FIGURE 3 for the context in which the branch units 302 are disposed and FIGURE 5 for details of the branch unit 302 components. Each first flag selector 504 presents a flag 508 from a plurality of available flags 25, 55 based upon contents in the flag selection memory 502. See Specification p. 21, lines 13-29. A second flag selector 506 accepts the flags 508 from the first flag selectors 504 and selects one of the flags 508 to present as a branch flag 304 based upon the branch condition address 300. See Specification p. 21, line 29 through p. 22, line 10. The branch flag 304 is a single bit that indicates to the sequencer whether to branch according to the conditional instruction. Because the programmable flag selection memory 502 is populated prior to test execution, processing in the first flag selector 504 occurs in parallel with the presentation of the branch condition address 300 to the second flag selector 506. The flags 508 are available to the second flag selector 506 at approximately the same time in the instruction cycle as the branch condition address 300. Determination of the branch state, therefore, occurs in a single instruction cycle and does not add latency to instruction processing. See Specification p. 22, lines 5-10. Also claimed is an

apparatus including a compiler that assigns appropriate values for the programmable flag selection memory 502 to pre-program the flags 508 that are available in a single test from all flags 25, 55 permitted by the tester. See Specification p. 23, lines 4 through p. 24, lines 10 and FIGURES 6 and 7.

Issues: I. Whether U.S. Pat. No. 5,991,868 to Kamiyama in view of U.S. Pat. No. 5,740,393 to Vidwans presents a prima facie case of obviousness with respect to claim 1?

II. Whether the combination of the Kamiyama and Vidwans patents and further in view of U.S. Pat. No. 4,742,466 to Ochiai presents a prima facie case of obviousness with respect to claim 15?

Grouping of Claims: Claims 1-11 stand and fall together. Claims 15-18 stand and fall together.

Argument:

I. A. The combination of the Kamiyama and Vidwans patents does not provide a prima facie case of obviousness with respect to claim 1 because neither Kamiyama nor Vidwans teaches "a programmable flag selection memory"...where..."each first flag selector presents[ing] a flag from a plurality of available flags based upon contents in said flag selection memory".

The Final Office Action maintains that the Kamiyama patent teaches a sequence of instructions including a conditional branch (Figure 6) and a branch unit (Figure 6, item 107) that selects flags 3,4 read out of a memory 106, which are used to determine a branch condition (col. 6, lines 49-67). See Paper No. 4, p. 3, paragraph 6, lines 4-7. Specifically, "a flag selecting means for selecting one of said plurality of flag storage means in accordance with an indication in a conditional branch instructions decoded by said instruction decoding unit". The Vidwans patent teaches a 2-stage multiplexer. See Paper No. 4 page 3, paragraph 6, lines 8-9 and page 10, last paragraph through page 11, line 6. The Final Office Action and Advisory Action maintain that the teachings of the Kamiyama patent may be combined with the teachings of the Vidwans patent to arrive at the invention of claim 1. The Advisory Action asserts that a flag selection memory is found in Vidwans (FIGURE 6 and col. 4, lines 48-52)[1] and that it would have been obvious to one of ordinary skill in the art to combine the sequencer and branch unit taught in the Kamiyama patent with a 2-stage multiplexer with a single flag bit as output in Vidwans. See Paper No. 7, p. 2, paragraph 2. In response, Applicant does not dispute that two stage multiplexors are known or that Vidwans

[1] The Office Action cites figure 6 of the Vidwans patent, but Applicant finds the 2-stage multiplexor in figure 9 of the Vidwans patent.

discloses a two-stage multiplexor in figure 9 of the drawings. Applicant's position is that the combination of Kamiyama and Vidwans does not teach or suggest a programmable flag selection memory where each first flag selector presents a flag based upon contents in said flag selection memory. As described in the Summary herein, use of the flag selection memory permits selection of some number of flags for use in a single test (32 in the disclosed embodiment) from a larger number of available flags in a logic tester, and does so with a minimum amount of hardware logic in the logic tester. See Specification p. 18, lines 15-18. No such disclosure or teachings of a relationship between a flag selection memory and a first stage of a multiple stage multiplexor is found in Kamiyama or Vidwans to suggest to one of ordinary skill in the art the desirability of a multiple stage multiplexer over the single stage multiplexer disclosed in Kamiyama. The compactness of the logic is even more apparent with respect to claim 2 where branch flags 304 from multiple branch units 302 are logically combined to create the branching bit. See figure 3 and Specification p. 24, line 21 through p. 25, line 2. The flag selection memory is programmed prior to test execution to select the appropriate flags 508 whose value, at the time of test execution, indicates whether the programmed condition is true or false. The ability to pre-program a subset of

flags 508 in the first stage of multiplexing obviates additional program latency in the condition assessment process. See Specification p. 22, lines 5-10. The second flag selector then selects the flag actually used in a particular instruction based upon the branch condition address programmed into the conditional branch instruction. See Specification p. 22, lines 1-3. It is Applicant's position that the mere addition of a two-stage multiplexor as taught in Vidwans to the conditional judging unit as taught in Kamiyama without the concept of the programmable flag selection memory and its influence on the flag selection process does sufficiently teach the invention of claim 1 for purposes of obviousness under 35 U.S.C. §103. A prima facie case of obviousness requires the combination of the cited references to contain all claimed elements and limitations. See MPEP §2143.03. Because the cited references do not teach or suggest the use of a programmable flag selection memory and its influence in the flag selection process, Applicant maintains that a prima facie case of obviousness is not presented in rejection of claim 1 and reversal of the final rejection is respectfully requested.

I.B. If the Board finds all claimed elements disclosed in the combination of cited references, a prima facie case of obviousness is not established because the

invention of claim 1 would not have been obvious to one of ordinary skill in the art because there is no suggestion in the cited references for a programmable flag selection memory that operates as an input to the first stage of a two stage multiplexor for selecting a flag from a plurality of available flags?

Presuming without admitting that all claim elements are disclosed in the cited references, a prima facie case of obviousness is not established because there is no suggestion or teaching in the art for combining the references to arrive at the invention of claim 1. See MPEP §2143.01. Without the suggestion in the art to support the combination, the combination amounts to impermissible hindsight reconstruction using the claim under examination as a guide. The test for whether there is an implicit showing is what the combined teachings, knowledge of one or ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. See In re Kotzab, 217 F. 3d 1365, 55 USPQ2d 1313 (Fed Cir. 2000). In determining the differences between the prior art and the claims, the question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. See MPEP §2141.02. The Final Office Action asserts that one of ordinary skill in the art would have been motivated to

combine the teachings of the Kamiyama and Vidwans patents "in order to provide a multiple stage input selector that would produce a single branching bit as a condition for a branch to be executed". The Final Office Action does not suggest why one of ordinary skill in the art would substitute a 2-stage multiplexor for a single stage multiplexor. The teachings in the present Specification teach a first stage that is addressed using pre-programmed values so that an output of the first stage is available to the second stage at the same time as the branch condition address so as to not add program latency into the conditional instruction execution time. See Specification p. 22, lines 4-10. Mere substitution of a dual stage multiplexor for the single stage multiplexor without a suggestion as to the selection method for the first stage of multiplexing does not sufficiently enable one of ordinary skill in the art to reproduce the invention of claim 1 and does not address one of the benefits found in the invention of claim 1. Accordingly, Applicant respectfully suggests that substitution of the 2-stage multiplexor taught in Vidwans for the single stage multiplexor taught in Kamiyama amounts to impermissible hindsight reconstruction using the present teachings as a guide. See In Re Mills, 916 F. 2d 680, 16 USPQ2d 1430 (Fed Cir. 1990). While it is not necessary to combine the cited references for the same reason as the Inventor, the

Office Actions also fail to find in the cited art any basis for the relationship between the recited element of a "programmable flag selection memory" and the single stage or multiple stage multiplexor and the "flag selected from a plurality of available flags" without reference to the present teachings. Accordingly, the rejection of claim 1 is not believed to be proper and reversal of the final rejection is respectfully requested.

II. The combination of the Kamiyama, Vidwans, and Ochiai patents does not provide a prima facie case of obviousness with respect to claim 15 because the cited references do not disclose a "compiler assigning ... values for a flag selection memory" and "a programmable flag selection memory"... where ... "each first flag selector presents[ing] a flag from a plurality of available flags based upon contents in said flag selection memory".

The combination of the Kamiyama, Vidwans and Ochiai patents does not disclose "a programmable flag selection memory, a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags based upon contents in said flag selection memory" where a compiler assigns "values for a flag selection memory" as claimed. Applicant asserts that claim 15 is patentable for the same reasons presented

herein that claim 1 is patentable because the Ochiai patent does not teach or suggest the programmable flag selection memory. The Advisory Action cites figure 4 and col. 3, lines 60-65 of Ochiai for the proposition that "the flag field is added to a conditional branch instruction and used as a value for the selection logic". Applicant does not dispute that it is known to program a conditional instruction with a value destined for selection logic inputs. Claim 15, however, recites a "compiler assigning ... values for a flag selection memory" in addition to "a branch condition address" as part of the conditional branch instruction, which is used as input to a second flag selector. The compiler of claim 15, therefore, assigns values destined for two different places. The Ochiai patent suggests values destined for the flag field of the conditional instruction to store information representing the execution history of the instruction. See Ochiai, col. 3, lines 1-12 and col. 3 line 60 through col. 4, line 7. This implies that the flag field is populated with a value both pre- and post-instruction processing. The pre-instruction processing value is always the "initial" state. The flag field value is not taught by Ochiai to be an input into a selector for presenting a flag from a plurality of available flags. The flag field execution history concept of Ochiai, therefore, does not teach or suggest a compiler assigning

values for the flag selection memory as claimed. In the present teachings, values programmed into the flag selection memory are available to the first flag selector as the conditional instruction is being processed. Accordingly, the teachings of adding a flag field to the conditional instruction do not teach or suggest "a compiler assigning ... values for a flag selection memory". Because the Ochiai reference discloses only that a flag field is added to a conditional branch instruction, it does not teach or suggest the presence or desirability of the programmable flag selection memory as programmed by the compiler and as used by the first flag selector. Because the flag field is part of the conditional branch instruction as taught in Ochiai, the flag field is available only after the conditional branch instruction is processed. Accordingly, the flag field as taught in Ochiai does not teach or suggest the programmable flag selection memory where programmed values are available prior to processing of the conditional branch instruction for purposes of selecting flags from available flags. In order for the combination to render a claim obvious, all elements and limitations must be taught or suggested by the prior art. See MPEP §2143.03. Because none of the cited references alone or in combination disclose the presence and desirability of the programmable flag selection memory and none of the cited references teach or

suggest the role of the compiler in assigning values for the flag selection memory, all elements and limitations found in claim 15 are not found in the combination of Kamiyama, Vidwans and Ochiai and a prima facie case of obviousness is not established. Accordingly, reversal of the final rejection is respectfully requested.

Respectfully submitted,

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Applicant(s)

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Appendix

1. An apparatus for conditional branching comprising:

a sequencer executing a plurality of program instructions, one or more of said program instructions including a conditional branch instruction, said conditional branch instruction specifying a branch condition address and a conditional instruction,

a branch unit comprising a programmable flag selection memory, a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags based upon contents in said flag selection memory, a second flag selector accepting a plurality of said flags and selecting one of said flags to present as a branch flag based upon said branch condition address, said branch flag indicating to said sequencer whether to branch according to said conditional instruction.

15. An apparatus for conditional branching comprising:

a compiler for converting source code including one or more conditional branch instructions into object code, the compiler assigning values for a branch condition address and values for a flag selection memory,

a sequencer executing said object code comprising one or more of said conditional branch instructions, each said conditional branch instruction specifying a branch condition address and a conditional instruction, and

a branch unit comprising a programmable flag selection memory, a plurality of first flag selectors,

each first flag selector presenting a flag from a plurality of available flags based upon contents in said flag selection memory, a second flag selector accepting a plurality of said flags and selecting one of said flags to present as a branch flag based upon said branch condition address, said branch flag indicating to said sequencer whether to branch according to said conditional instruction.